REMARKS

Claims 1-24 are pending. Claims 1-14 are allowed. Claims 18 and 22 are rejected under 35 U.S.C. § 112, second paragraph. Claims 15-24 are rejected under 35 U.S.C. § 103(a). Claims 18, 20, and 22 are currently amended.

The drawings are objected to as failing to comply with 37 C.F.R. § 1.84(p)(5) because of reference numerals 814, 834, 850, and 862 are not mentioned in the description. Reference numeral 814 is mentioned at page 15, line 20. Reference numeral 850 is mentioned at page 13, line 3. The paragraph at page 12, line 19 has been amended to mention reference numeral 834. The paragraph at page 16, line 9 has been amended to mention reference numeral 862.

The drawings are further objected to as failing to comply with 37 C.F.R. § 1.84(p)(5) because –Vmax (page 3, line 1) is not shown at Figure 2. The paragraph at page 2, line 21 has been amended to delete the reference to –Vmax. Thus, applicant believes the present amendment to the specification overcomes the drawing objection under 37 C.F.R. § 1.84(p)(5).

Claim 18 is rejected under 35 U.S.C. § 112, second paragraph, because N is not clearly defined. Claim 18 is amended to define N as a positive integer. In a preferred embodiment of the present invention shown at Figure 8 and described at page 9, line 27 through page 10, line 6, N is 5 and 2^N is 32. Applicant believes the present amendment adequately defines N. Thus, claim 18 is patentable under 35 U.S.C. § 112, second paragraph.

Claim 22 is rejected under 35 U.S.C. § 112, second paragraph, because there is no antecedent for "the address table." Claim 22 is amended to recite "an address table." Thus, claim 22 is patentable under 35 U.S.C. § 112, second paragraph.

Claims 15-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Rao (U.S. Pat. No. 6,041,389). Claims 15-19 define a very specific structure of the present invention as

shown at Figure 8 and described at page 9, line 21 through page 11, line 12. In particular, claims 15-19 recite "an address table (A0-Am) arranged to store a plurality of addresses and coupled to receive an external address (from bus 870); a data table (D0-Dm) coupled to the address table and arranged to store a first plurality of data words (CAM 602 includes a 32-word address table A0-Am and a corresponding 32-word data table D0-Dm, page 9, lines 22-23), each data word corresponding to a respective address in the address table; a nonvolatile memory circuit (Figure 7) arranged to store a second plurality of data words (6 Mbit FRAM array 710 is organized as 196,608 32-bit words, page 9, line 2) greater than the first plurality; and a data terminal coupled to the data table and to the nonvolatile memory circuit." (reference numerals added). The invention of claims 15-19 advantageously routes multiple memory accesses to a same memory address to data table 840 (Figure 8) rather than to the FRAM array 710 (Figure 7). This greatly reduces fatigue of the FRAM array.

Rao fails to teach or suggest these features or the corresponding advantages. Rao discloses (Figure 2) a multibank memory (Bank 0 through Bank X) that may be configured for individual access or parallel access by writing a Bank Select address into each CAM array 207 at system initialization. (col. 6, lines 38-51). Examiner states "Input/output circuitry 213 obviously including address table to store addresses . . . data table to store data words . . . and providing all control signal and system clocks to control the system." Office Action 4/1/05, page 4, paragraph 6). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Here, the limitations of claims 15-19 are simply not disclosed by Rao. There is no address table or corresponding data table. There is not even a reason to think there might be an address table or corresponding data table, since the invention of Rao is directed to a completely different purpose. Thus, applicant respectfully submits that claims 15-19 are patentable under 35 U.S.C. § 103(a) over Rao.

Claims 20-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Rao. Claims 20-24 define a very specific structure of the present invention as shown at Figures 6-8 and described at page 7, line 3 through page 11, line 12. In particular, claims 20-24 recite "a nonvolatile memory circuit (Figure 7) arranged to store a first data word (same as D0) at a first address (same as A0); a volatile memory circuit (D0-Dm) arranged to store the first data word (D0) and the first address (A0); a data bus (610 Figure 6) coupled to the processor and the volatile and nonvolatile memory circuits; and an address bus (608 Figure 7) coupled to the processor and the volatile and nonvolatile memory circuits." (reference numerals added). These features of the present invention are simply not disclosed by Rao. If data stored in memory array 202 of Rao (Figure 2) is taken as "a first data word" of claims 20-24, there is no corresponding volatile memory circuit to store the same "first data word" as required by claims 20-24. CAM array 207 only stores Bank Select address bits. (col. 6, lines 39-41). Thus, applicant respectfully submits that claims 20-24 are also patentable under 35 U.S.C. § 103(a) over Rao.

In view of the foregoing, applicant respectfully requests approval or the present amendment, and reconsideration and allowance of claims 1-24. If the Examiner finds any issue that is unresolved, please call applicant's attorney by dialing the telephone number printed below.

Respectfully submitted,

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